EE619: Project-II

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Design for Cross-coupled Oscillator

In order to limit the power below 3mW, we can take I to be $\mathbf{2mA}$. Say we choose $L_1 = L_2 = 1$nH (if we use a centre-tapped inductor: $\boldsymbol{L = 2nH}$). The oscillation frequency is given as follows:

$$2\pi \times f_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{var})}}$$

For an oscillation frequency of 6GHz, we get $C_1 + C_{var} = 700fF$. Say we choose $\boldsymbol{C_{var} = 20fF}$ and $\boldsymbol{C_1 = C_2 = 680fF}$.

We can choose a width $\boldsymbol{W = 3200nm}$ for M_0 and M_1 in order to get nearly complete current switching with V_{swing}.

In order to scale I_{BIAS} to I requires a width ratio of $I/I_{BIAS} = 10$. Therefore we can use $\boldsymbol{W = 10\mu m}$ and $\mathbf{1}\boldsymbol{\mu m}$ for M_2 and M_3 respectively.

Table 1 summarizes the final component parameters used. Figure 1 shows the schematic of the VCO along with component parameter annotations and 2 shows the schematic for the testbench used.

MOS Devices	**Finger Width**	**Length**	**Multipliers**	**Fingers**
M_0	800nm	60nm	1	4
M_1	800m	60nm	1	4
M_2	5μm	60nm	1	2
M_3	500nm	60nm	1	2
Passive Components				**Value**
L				2nH
C_0				20fF
C_1				20fF
C_2				501fF
C_3				501fF
I_{BIAS}				200μA
V_{DD}				1.2V

Table 1: Component parameters used for the VCO.

1 Schematic

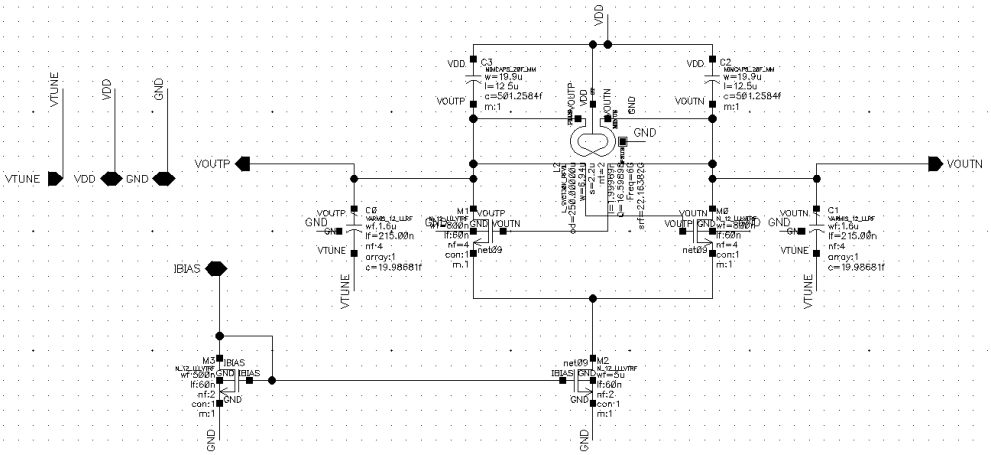


Figure 1: Schematic for the VCO with component parameter annotations.

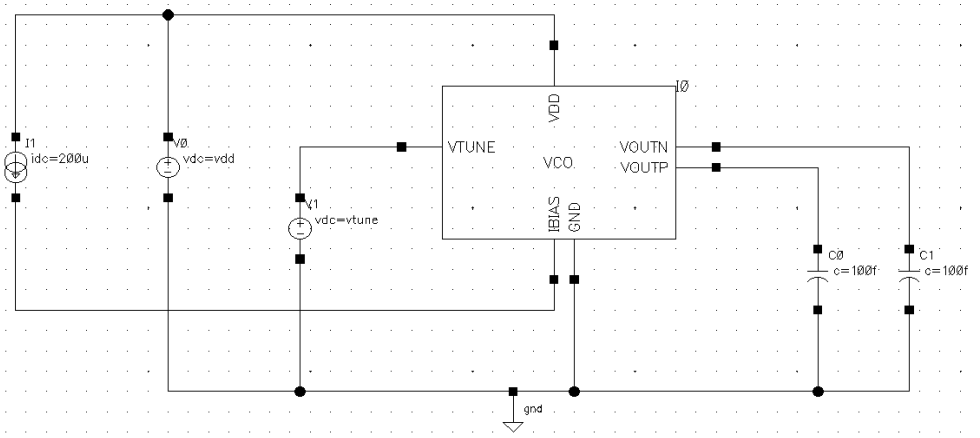
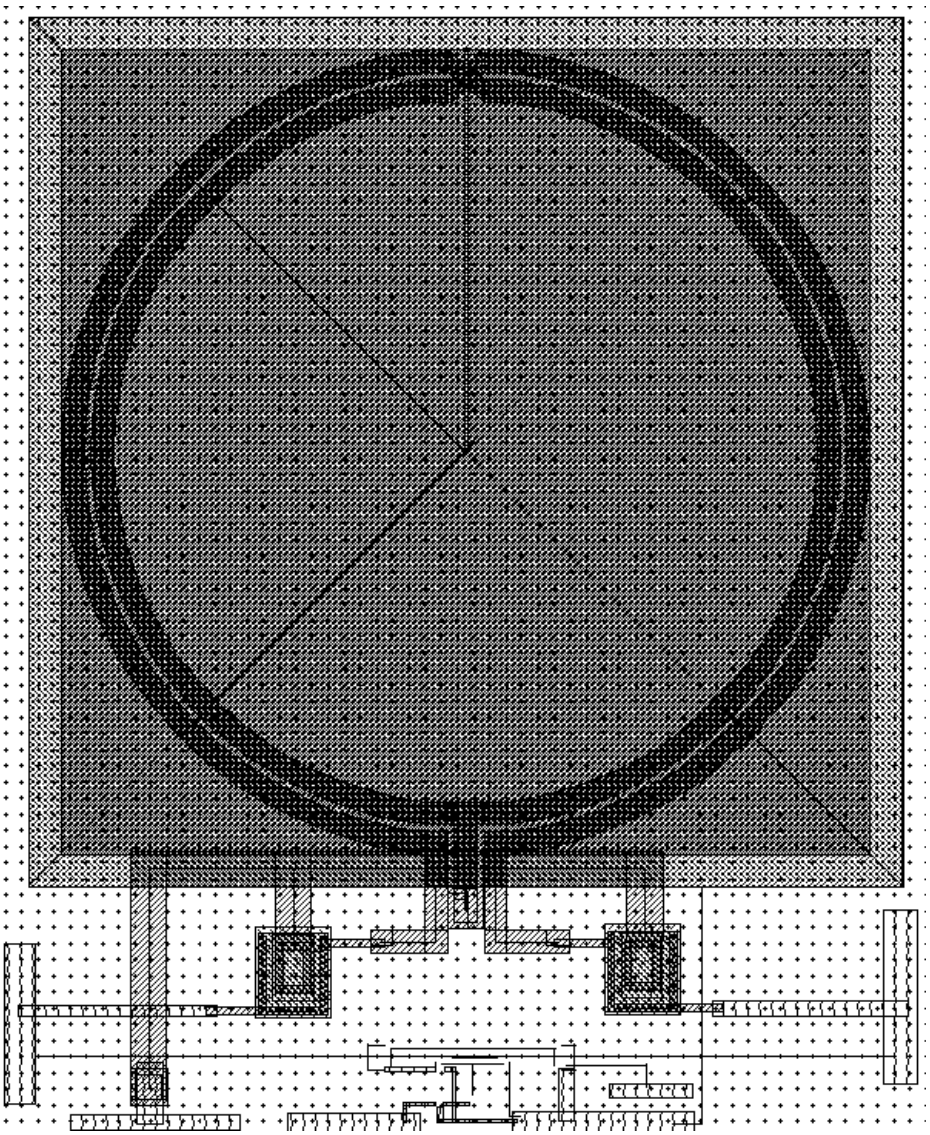
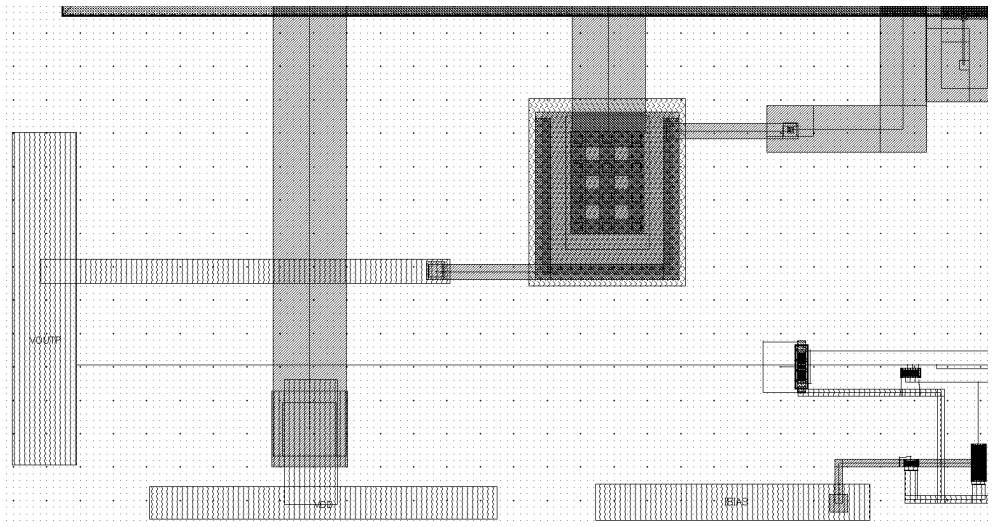
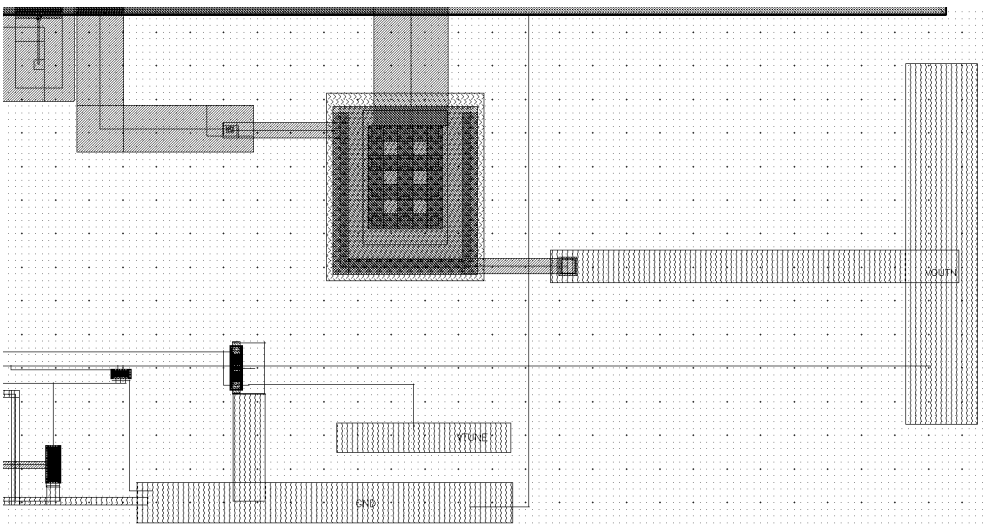


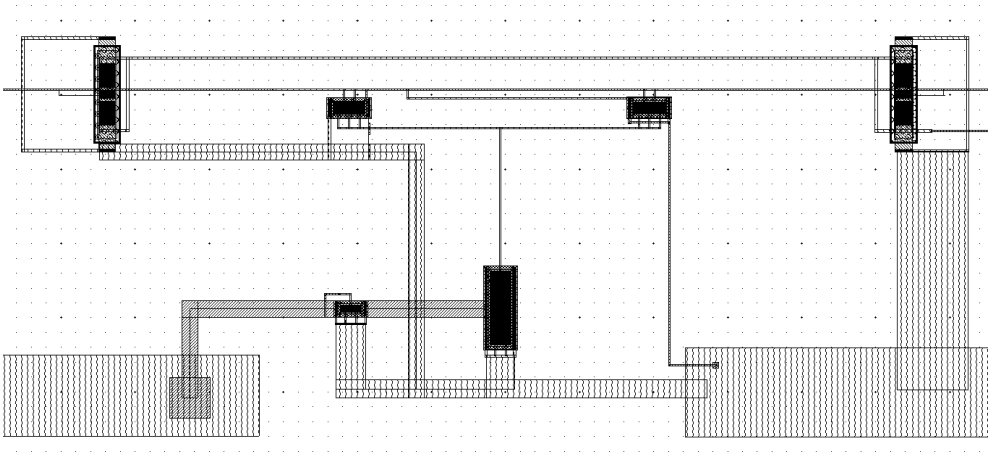
Figure 2: Schematic for the VCO testbench.

2 Layout

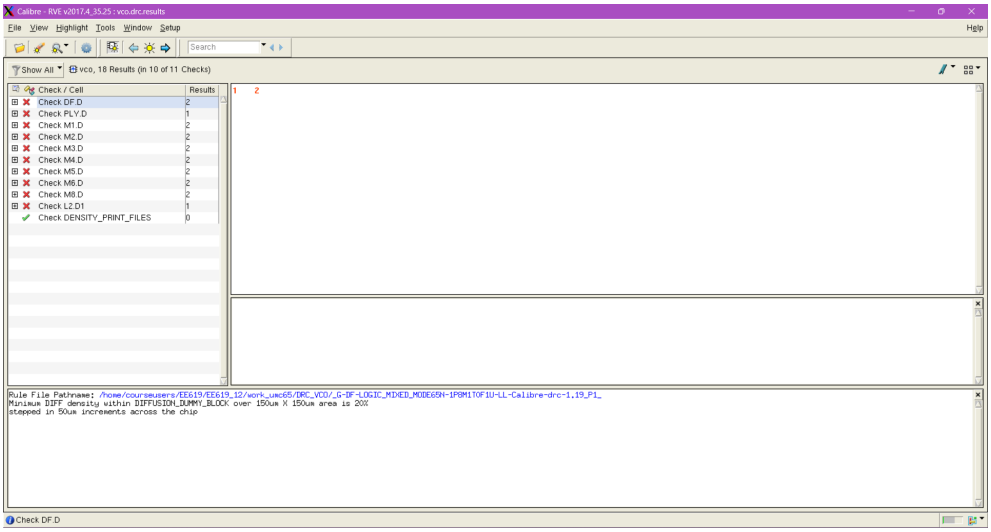



VOUTP
VBP
BIAS

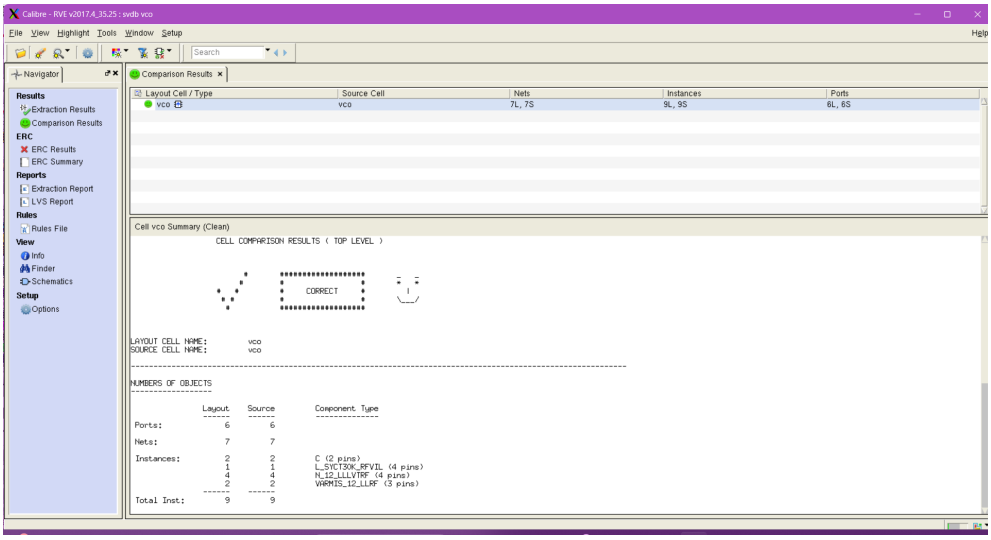

VOUTN
VTUNE
GND



3 DRC


Calibre - RVE v2017.4_35.25 : vco.drc.results
File View Highlight Tools Window Setup
Help
Search
Show All
vco, 18 Results (in 10 of 11 Checks)
Check / Cell
Results
Check DF.D 2
Check PLY.D 1
Check M1.D 2
Check M2.D 2
Check M3.D 2
Check M4.D 2
Check M5.D 2
Check M6.D 2
Check M8.D 2
Check L2.D1 1
Check DENSITY_PRINT_FILES 0
1 2
Rule File Pathname: /home/courseusers/EE619/EE619_12/work_uwc65/DRC_VCO/_G-DF-LOGIC_MIXED_MODE65N-1P8M1TOF1U-LL-Calibre-drc-1.19_P1_
Minimum DIFF density within DIFFUSION_DUMMY_BLOCK over 150um X 150um area is 20%
stepped in 50um increments across the chip
Check DF.D

4 LVS


Calibre - RVE v2017.4_35.25 : svdb vco
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Extraction Results
Comparison Results
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
vco
vco
7L, 7S
9L, 9S
6L, 6S
Cell vco Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: vco
SOURCE CELL NAME: vco
NUMBERS OF OBJECTS
Layout
Source
Component Type
Ports: 6 6
Nets: 7 7
Instances: 2 2 C (2 pins)
1 1 L_SYCT30K_RFVIL (4 pins)
4 4 N_12_LLVTRF (4 pins)
2 2 VARMIS_12_LLRF (3 pins)
Total Inst: 9 9

5 Transient

Figure 3 shows the transient signal at the output node of the designed VCO. Here, we can see that we have a peak-to-peak voltage swing of around $\mathbf{1.083}\boldsymbol{V_{pp}}$, which meets the required specification.

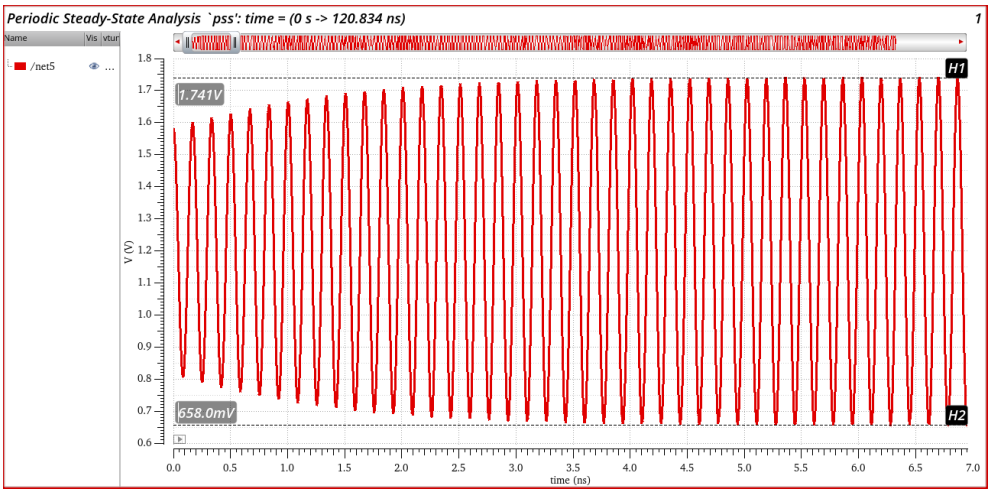

Figure 3: Transient signal at the output node of the VCO.

6 Frequency Tuning

Figure 4 shows the variation of oscillator frequency as V_{tune} varies from 0 to 1.2V. We can observe a tuning range of about **28MHz**. We also observe a max K_{VCO} value of around $\mathbf{61MHz/V}$, which is within the required specification. From the schematic simulations, we can observe that the oscillation frequency at $V_{TUNE} = 0.6V$ is around **6.3GHz** and the tuning range is higher, at around **32MHz**. This is because of parasitic capacitances considered in the post-layout simulations, which reduce the oscillation frequency and the tuning range.

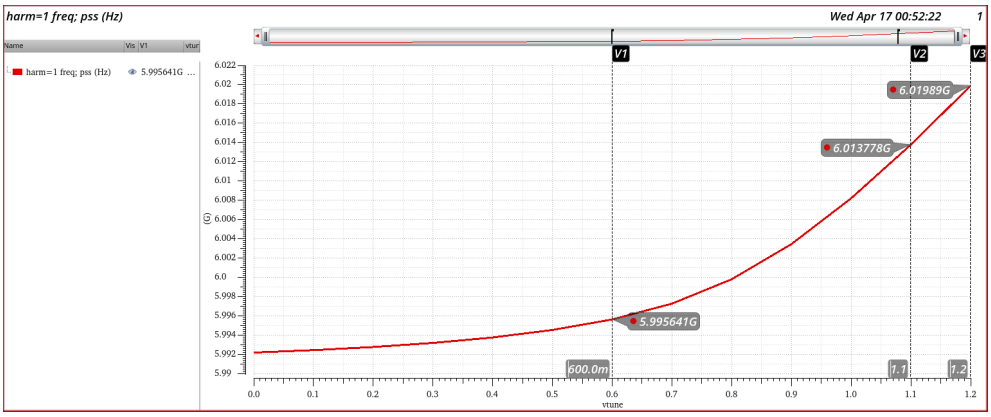

Figure 4: Plot for frequency as V_{tune} varies in post-layout simulations.

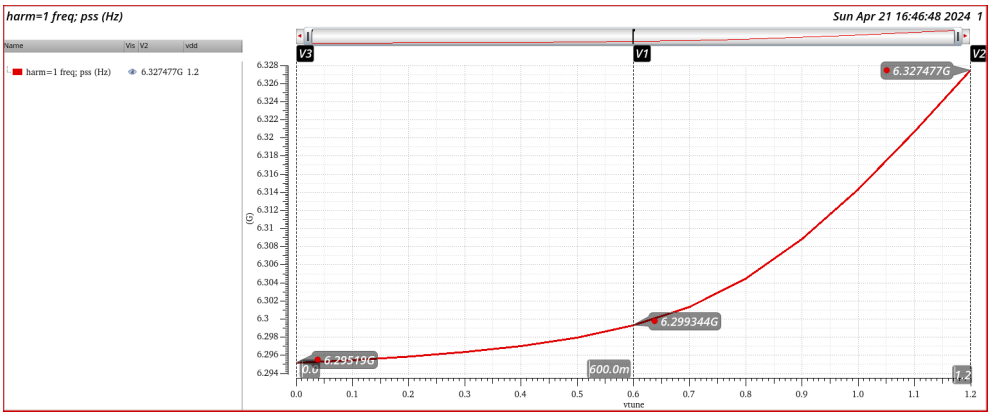

Figure 5: Plot for frequency as V_{tune} varies in schematic simulations.

7 Phase Noise

Figure 6 shows the phase noise (in dBc) for the designed LNA circuit. The phase noise at a relative frequency of 1MHz is close to $\mathbf{-117dBc/Hz}$, which meets the desired specification.

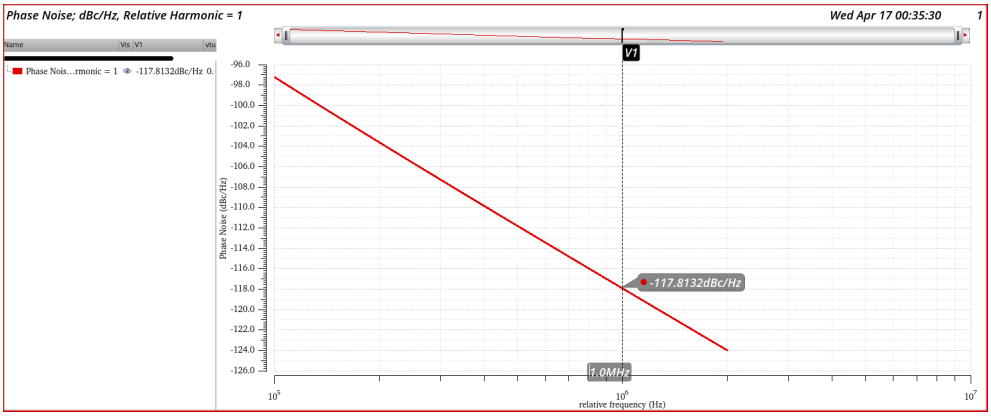

Figure 6: Phase Noise (in dBc) for the designed VCO circuit.

8 Variation with V_{DD}

Figure 7 shows the variation of oscillator frequency as V_{tune} varies from 1.0 to 1.4V. As we increase V_{DD}, the V_{GS} of the varactors M_2, M_3 increases. Due to this the capacitance of the varactors also increases as we increase V_{DD}. This leads to a decrease in the oscillation frequency.

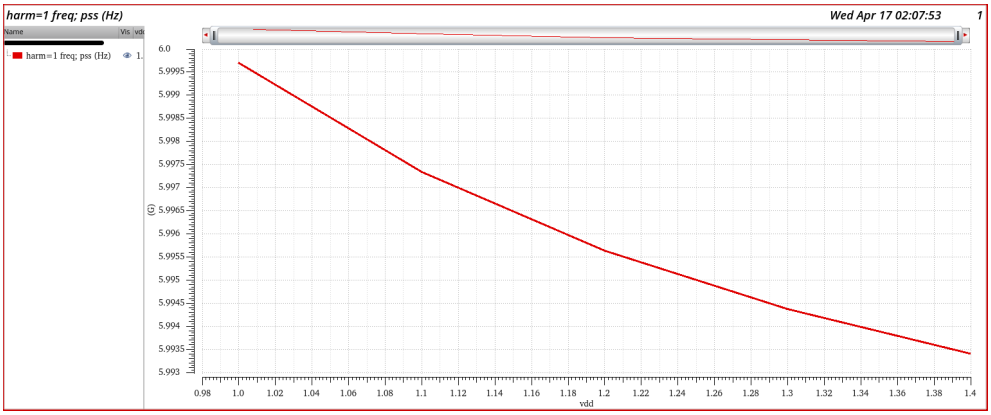

Figure 7: Plot for frequency as V_{DD} varies.