EE618: Project

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1 Hand Calculations

We calculate the constant $K = \mu C_{ox}$ for the 3 different MOSFET devices. Figure 1 shows the $\beta_{eff} = K \times (W/L)$ values. Using this we calculate the following:

$$K_{n,nat} = 311.7\mu A/V^2$$
$$K_{n,lvt} = 247.5\mu A/V^2$$
$$K_{p,lvt} = 201.8\mu A/V^2$$

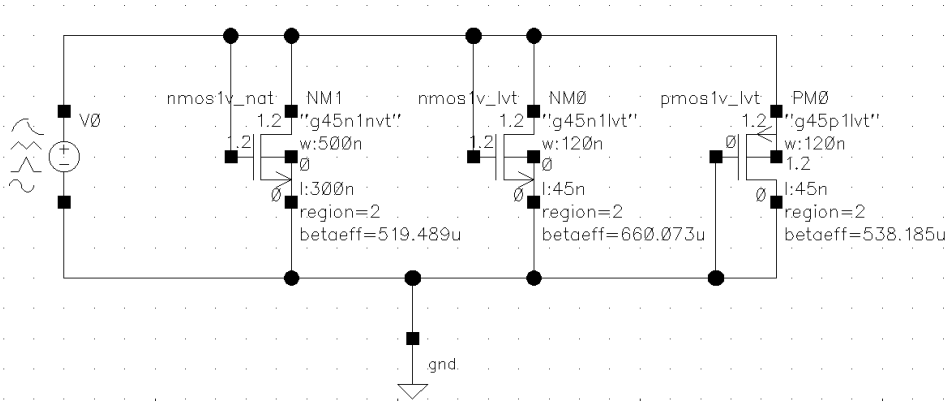

Figure 1: β_{eff} values for NAT nMOS, LVT nMOS, and LVT pMOS.

We know that the noise characteristics of a 2-stage OTA are given as:

$$\overline{V_{n,eq}^2} = \frac{16kT}{3 \times g_{m_1}}[1 + \frac{g_{m_3}}{g_{m_1}}]$$

Assuming $g_{m_3} \ll g_{m_1}$, the required noise characteristics give us the following inequality:

$$g_{m_1} \geq \frac{16kT}{3} \times \frac{1}{80nV/\sqrt{\text{Hz}}} = 3.45\mu S$$

The unity-gain frequency is given by:

$$f_{UGF} = \frac{g_{m_1}}{2\pi C_C}$$

Since we want $f_{UGF} \geq 70MHz$, we get the following inequality:

$$C_C \geq 0.008pF$$

Say we use $C_C = 0.1pF$. The current I_{SS} is given by

$$I_{SS} = C_C \frac{dV_{out}}{dt} = C_C \times (\text{Slew Rate}) \geq 7\mu A$$

Using this, we get the following inequality for I_{OSS}:

$$I_{OSS} \geq I_{SS}(1 + \frac{C_L}{C_C}) \geq 77\mu A$$

Say we use $I_{SS} = 26.23\mu A$, $I_{OSS} = 151.28\mu A$, and $g_{m_1} = 84\mu S$. Using this we calculate the (W/L) for M1 as follows:

$$(W/L)_1 = \frac{g_{m_1}^2}{K_{n,nat} \times I_{SS}} = 0.86$$

Using the above values, we get $f_{UGF} = 133$MHz. The phase margin is approximately given by

$$P \cdot M \cdot = 90^\circ - tan^{-1}(\frac{f_{UGF}}{f_{ND}})$$

Therefore we get

$$f_{ND} = \frac{g_{m_6}}{2\pi C_L} \geq 230\text{MHz}$$

This gives us $g_{m_6} \geq 1.445mS$. Say we choose $g_{m_6} = 2mS$,

$$(W/L)_6 = \frac{g_{m_6}^2}{2 \times K_{p,lvt} \times I_{OSS}} = 65$$

The value of the resistor is given by

$$R_z = \frac{1}{g_{m_6}}(1 + \frac{C_L}{C_C}) = 5.5k\Omega$$

To obtain a voltage swing of $0.6V_{pp}$, therefore $V_{dsat_6} = V_{dsat_7} = 300mV$

$$V_{dsat_6} = \sqrt{\frac{2I_{OSS}}{K_{p,lvt}(W/L)_6}} = 150mV$$

$$(W/L)_7 = \frac{2I_{OSS}}{K_{p,lvt} \times V_{dsat_7}^2} = 16$$

For zero systemic offset,

$$(W/L)_{3,4} = \frac{I_{SS}}{2I_{OSS}}(W/L)_6 = 3$$

The gain of the OTA is given by:

$$A_v = A_{v_1} \cdot A_{v_2} = \frac{\sqrt{\frac{8 \times K_{p,lvt} \times K_{n,nat} \times (W/L)_1 \times (W/L)_6}{I_{SS} \times I_{OSS}}}}{(\lambda_{n,nat} + \lambda_{p,lvt})(\lambda_{n,lvt} + \lambda_{p,lvt})}$$

Using $\lambda_{n,nat} = \lambda_{p,lvt} = \lambda_{n,lvt}$, we get

$$\frac{84.2}{4\lambda^2} \geq 250$$

Therefore, we get $\lambda \leq 0.29$. Suppose we take $\lambda_{n,nat} = \lambda_{p,lvt} = \lambda_{n,lvt} = 0.05$. Using the relation $\lambda \cdot L =$ constant, and the given λ values, we get the following lengths:

$$L_{n,nat} = 4.2\mu m$$
$$L_{n,lvt} = 600nm$$
$$L_{p,lvt} = 400nm$$

Table 1 summarizes the final component parameters used. Figure 2 shows the schematic of the OTA along with component parameter annotations.

MOS Device Parameters	Width (in μm)	Height (in μm)
NM1	3	4.2
NM2	3	4.2
PM3	4	0.4
PM4	4	0.4
NM5	2	0.6
NM6	24	0.4
NM7	9	0.6
NM3	0.7	0.6
Passive Components		**Value**
R0		$6.4k\Omega$
C0		$0.1pF$

Table 1: Component parameters used for the 2-stage OTA.

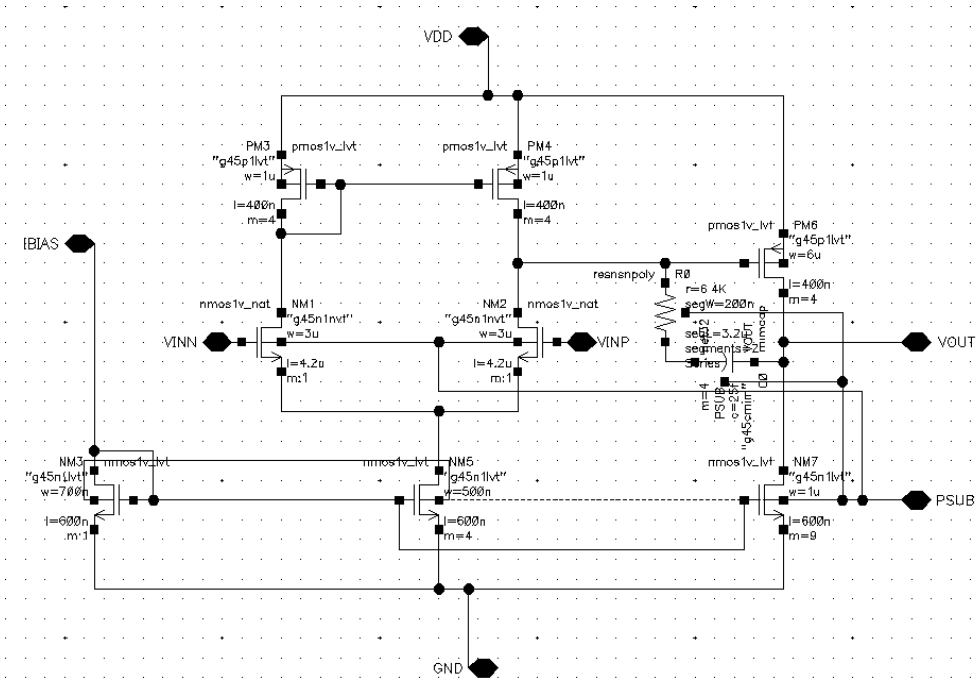

Figure 2: Schematic with component parameter annotations.

2 DC Operating point

Figure 3 shows the DC Operating point values for all the MOSFETs used. Here, we can see that all the MOSFETs are in region 2, i.e., saturation.

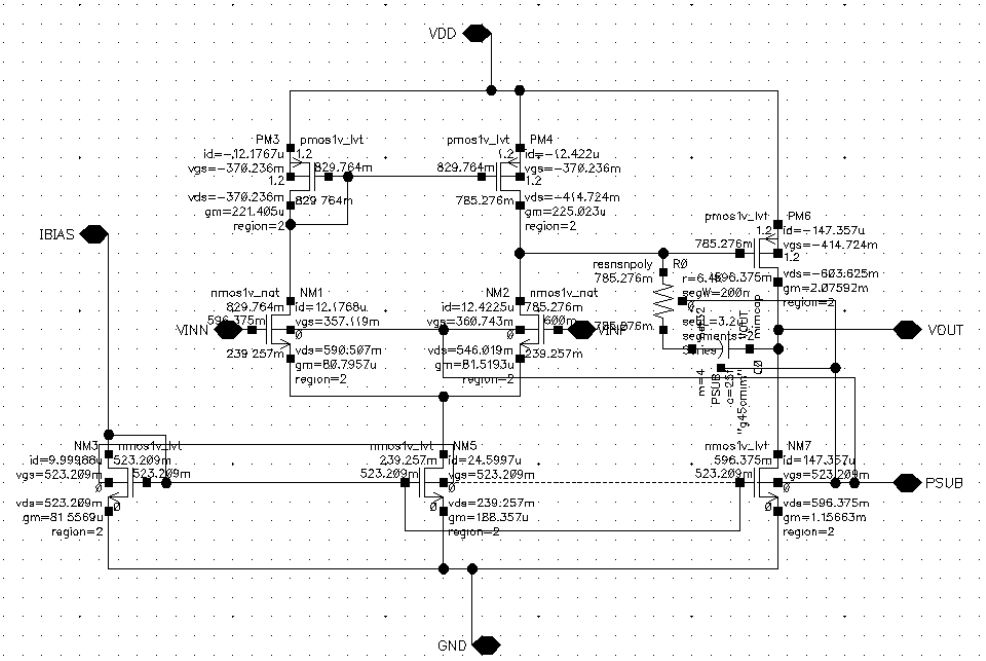

Figure 3: Schematic with DC operating point annotations.

The power consumption can be given by

$$\text{Power} = V_{DD} \times (I_{BIAS} + I_{SS} + I_{OSS}) = 1.2V \times 182\mu A = 0.218mW$$

3 Stability Analysis

Figure 4 shows the Bode plot for Gain and Phase. Here, we can observe a **DC Gain of 50.4dB**, a **3dB frequency of around 355kHz**, a **unity gain frequency of 116MHz**, and a **phase margin of around** 68.5°. Figure 5 shows the summary of the stability analysis.

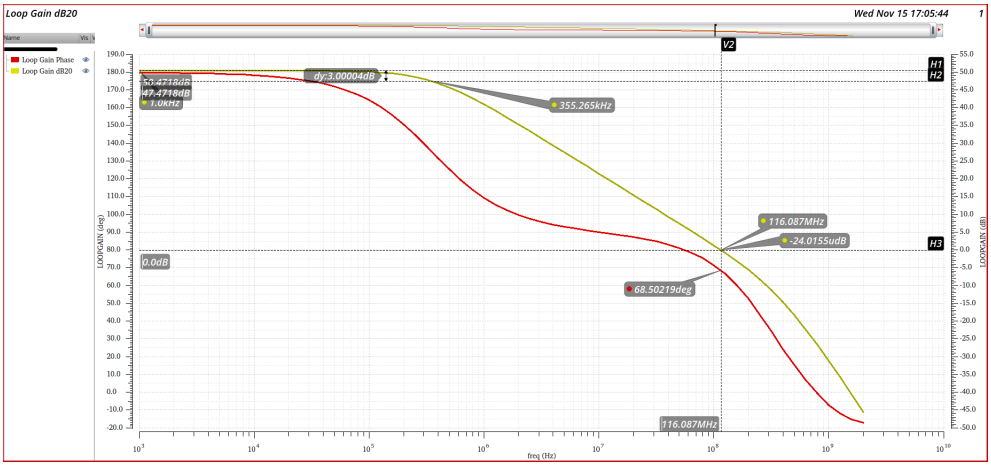

Figure 4: Bode Plots for Gain and Phase.

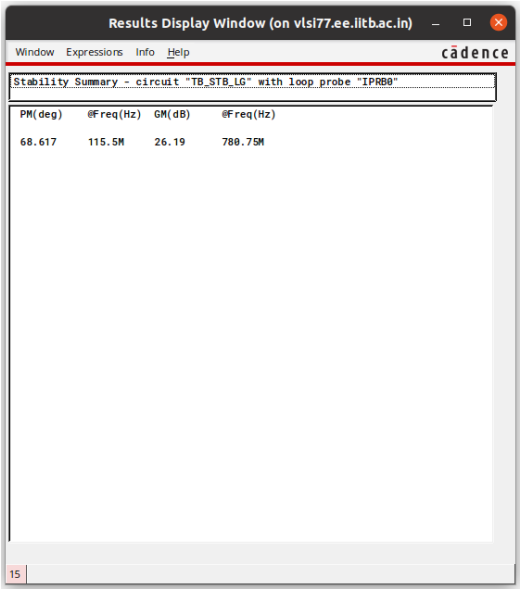

Figure 5: Stability summary.

4 AC Analysis: Differential gain

Figure 6 shows the plot for closed-loop gain and phase. We can observe the **closed-loop gain of around -7mdB** and a **3dB frequency of around 174MHz**. Figure 7 shows an **input referred systematic offset of 3.208m**. Figure 8 shows the DC Operating point values for all the MOSFETs used. Here, we can see that all the MOSFETs are still in saturation.

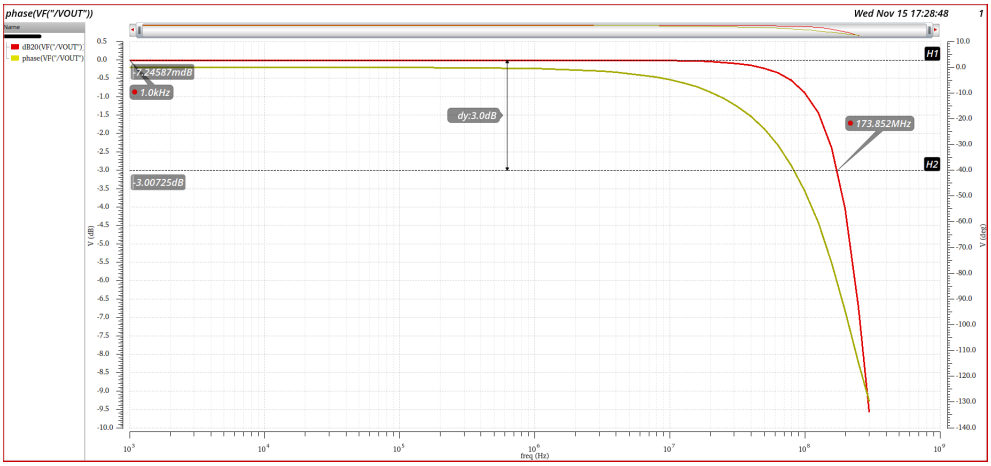

Figure 6: Bode Plots for Closed-loop Gain and Phase.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_200070008:TB_AC_DM:1	dB20(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_DM:1	phase(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_DM:1	Input reffered offset	3.208m			

Figure 7: Input referred systematic offset.

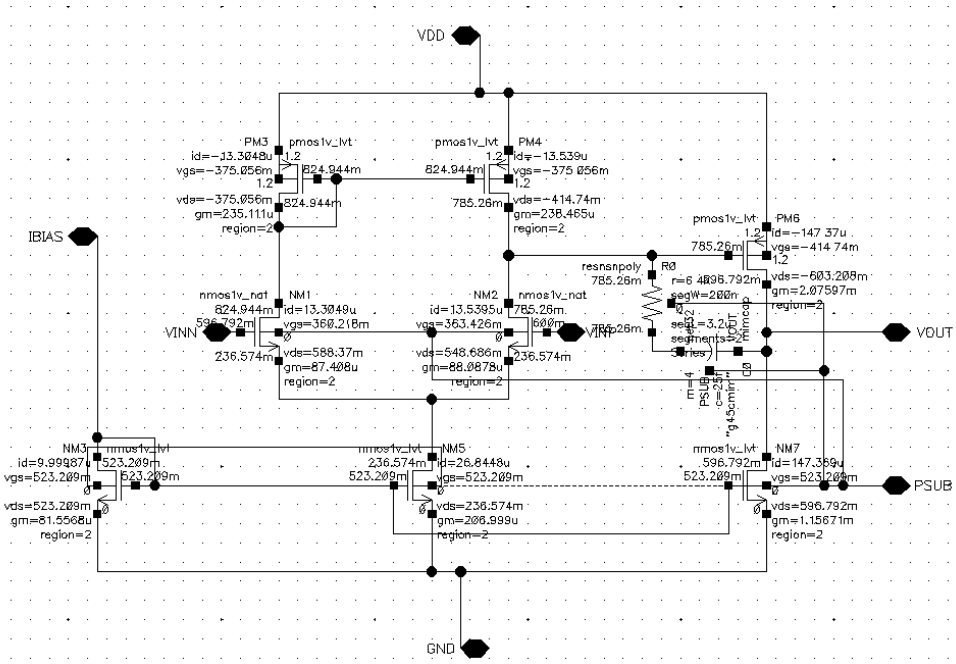

Figure 8: Schematic with DC operating point annotations.

5 DC Analysis: Common mode gain

Figure 9 shows the Bode plot for open-loop common-mode gain and phase. Figure 10 shows that the OTA has common-mode gain $A_{CM,dB} = -18.6dB$

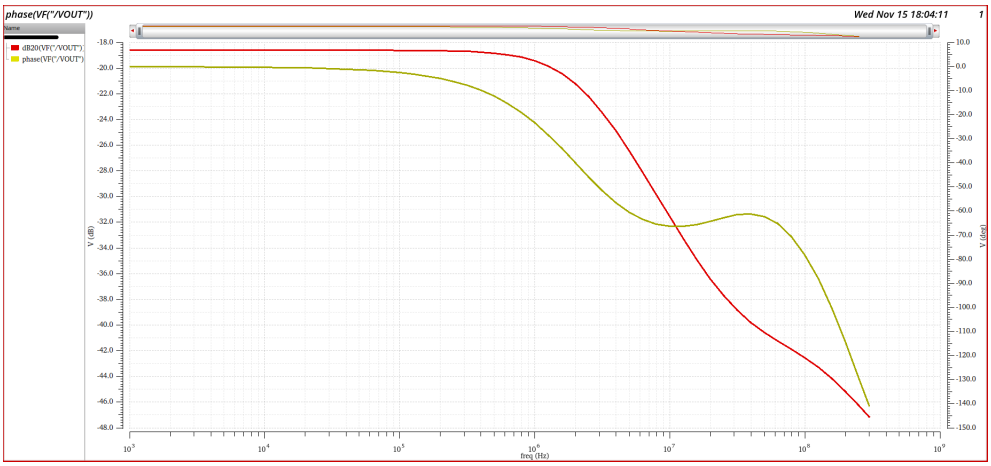

Figure 9: Bode Plots for Open-loop Common-mode Gain and Phase.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_200070008:TB_AC_CM:1	dB20(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_CM:1	phase(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_CM:1	ACM (in dB)	-18.6			

Figure 10: Common-Mode Gain.

The CMRR of the OTA is given by

$$\text{CMRR} = A_{DM,dB} - A_{CM,dB} = 50.4dB - (-18.6dB) = 69dB$$

6 Transient Analysis: Sinusoidal input

Figure 13 shows the plot for the input and output waveforms for the OTA. Figure 12 shows that the peak-to-peak voltage for the output waveform is around **596mV**.

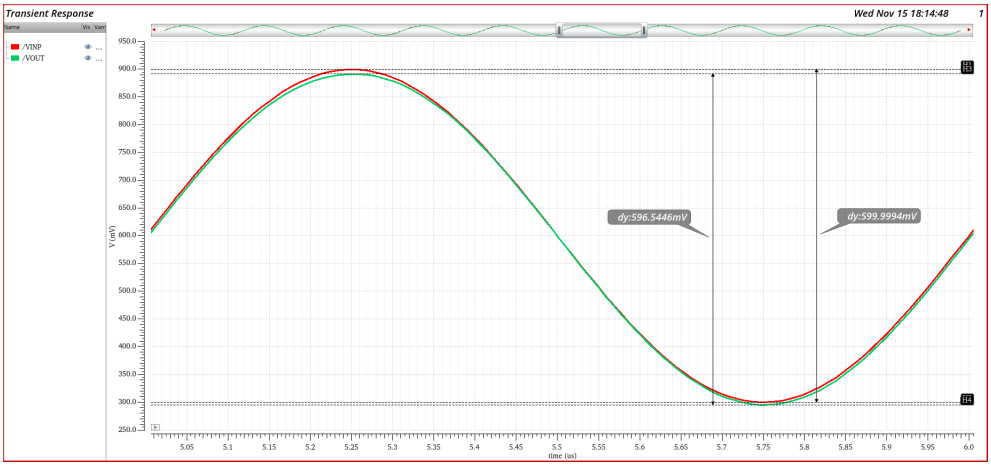

Figure 11: Plots for input and output transient waveforms.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20007 0008:TB_TRAN_SIN:1	/VOUT				
EE618_CP1_20007 0008:TB_TRAN_SIN:1	/VINP				
EE618_CP1_20007 0008:TB_TRAN_SIN:1	VOUT (peak-peak)	596.1m			
EE618_CP1_20007 0008:TB_TRAN_SIN:1	VIN (peak-peak)	600m			

Figure 12: Peak-to-peak voltage for input and output waveforms.

7 Transient Analysis: Step input

Figure 13 shows the plot for the input and output waveforms for the OTA to observe slewing. The slew rate is given by the following:

$$\text{Slew Rate} = \frac{\Delta V}{\Delta t} = \frac{14.36mV}{0.083ns} = 173V/\mu s$$

The settling time can be observed to be around **5.06ns**.

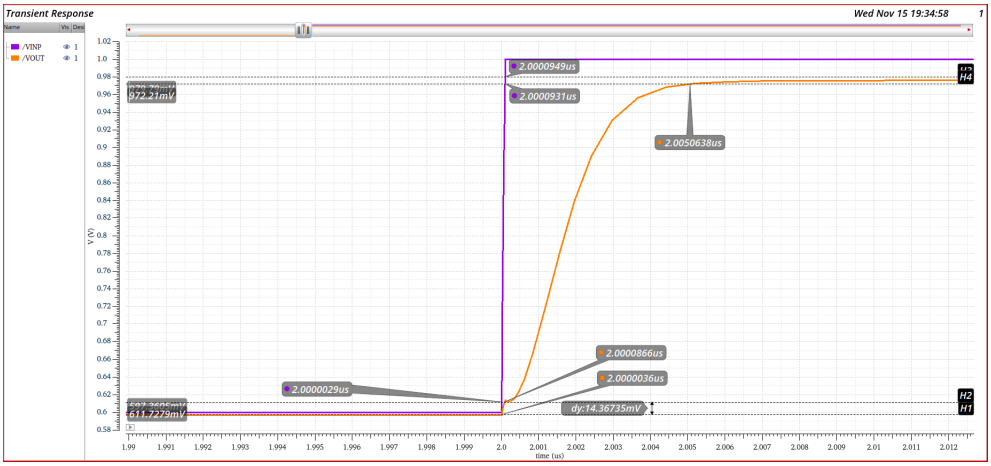

Figure 13: Plots for input and output transient waveforms to observe slewing.

8 Noise Analysis

Figure 14 shows the plot for the noise waveform. We can observe that for 1MHz, we have $\overline{V_{n,in}} = 34.5nV/\sqrt{\text{Hz}}$ and $\overline{V_{n,in}} = 30.8nV/\sqrt{\text{Hz}}$ for 10MHz frequency. Figure 15 shows the summary of the noise analysis.

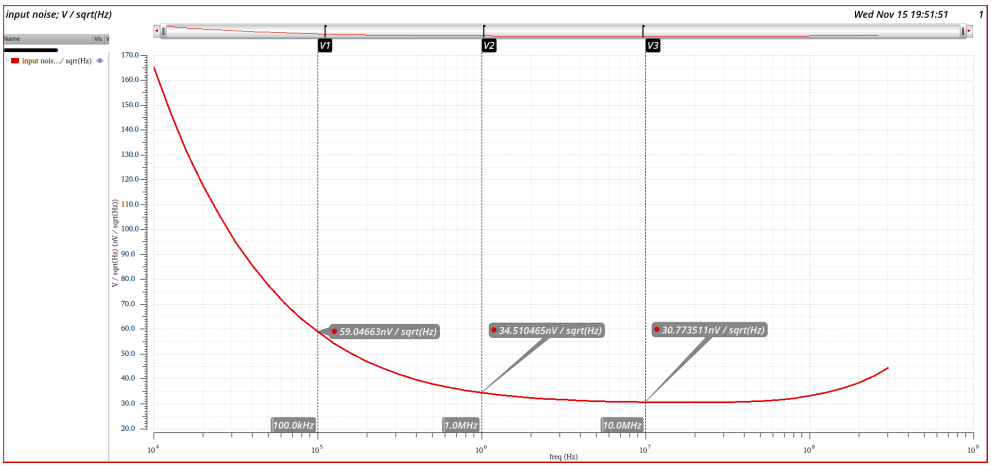

Figure 14: Plots for noise waveform.

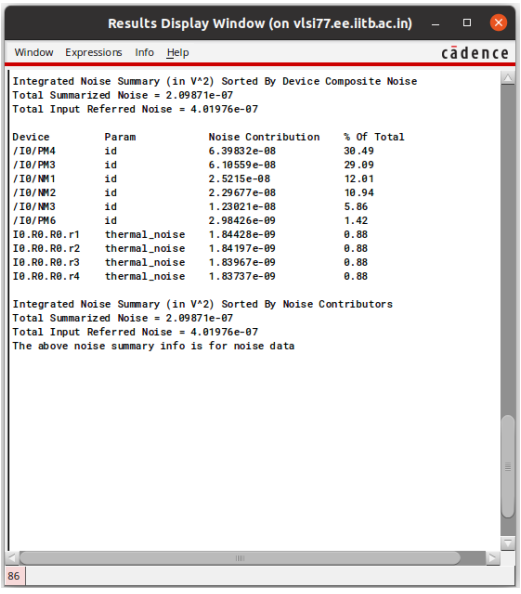

Figure 15: Noise summary.

Q. No.	Parameters	Value
2	Power Consumption	0.218mW
3	DC Gain	50.4dB
	f-3dB	355kHz
	Unity gain frequency	116MHz
	Phase Margin	68.5°
4	Closed loop Gain	-7mdB
	f-3dB	174MHz
	Input referred offset	3.208m
5	Common mode gain	-18.6dB
	CMRR	69dB
6	Output Swing	596mV
7	Slew rate	$173V/\mu s$
	Settling time	5.06ns
8	Input referred spot noise (at 1MHz)	$34.5nV/\sqrt{Hz}$
	Input referred spot noise (at 10MHz)	$30.8nV/\sqrt{Hz}$
	Total summarized noise	2.1×10^{-7}
	Total input referred noise	4.02×10^{-7}

Table 2: Summary of the OTA specifications.

9 Layout

Figure 16 shows the final layout of the designed OTA.

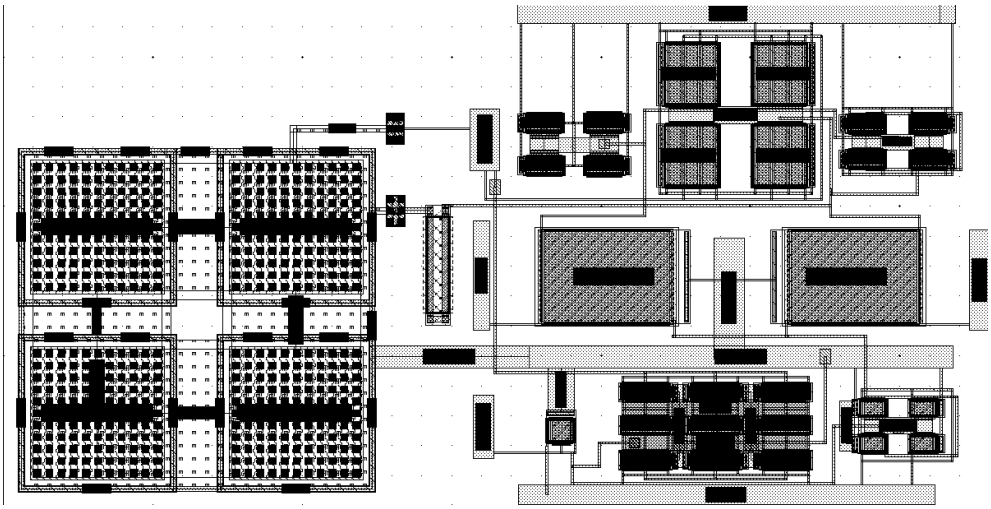

Figure 16: Layout of the designed OTA.

The layout dimensions are $33\mu m \times 17\mu m$, leading to a total area of $561\mu m^2$.

10 DRC, LVS, and QRC

Figure 17 shows that the OTA layout passes all DRC checks.

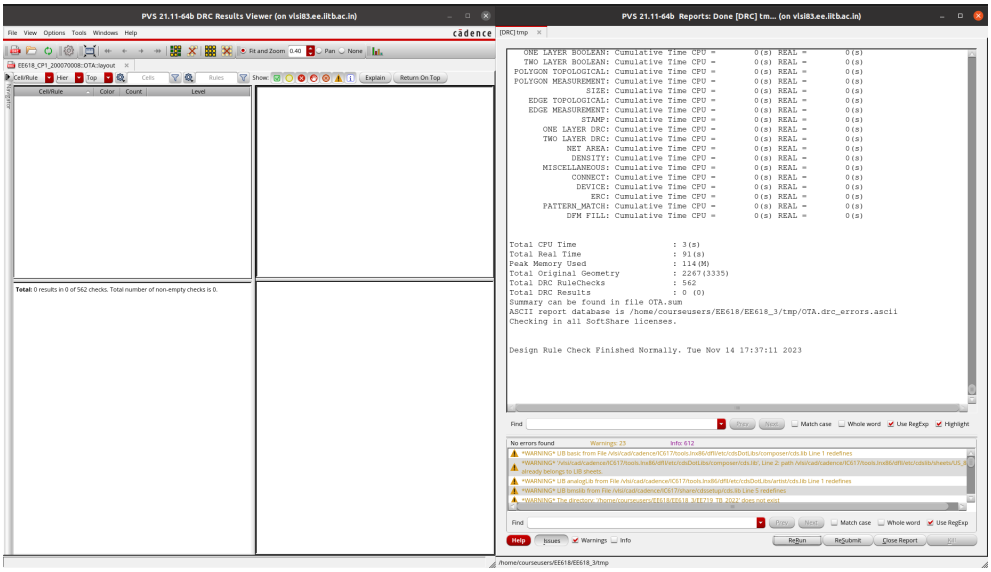

Figure 17: DRC checks for the OTA layout.

Figure 18 shows that the OTA layout passes all LVS checks with a few warnings.
Figure 19 shows that the Quantus Run was successful.
Figure 20 shows the OTA layout after parasitic extraction.

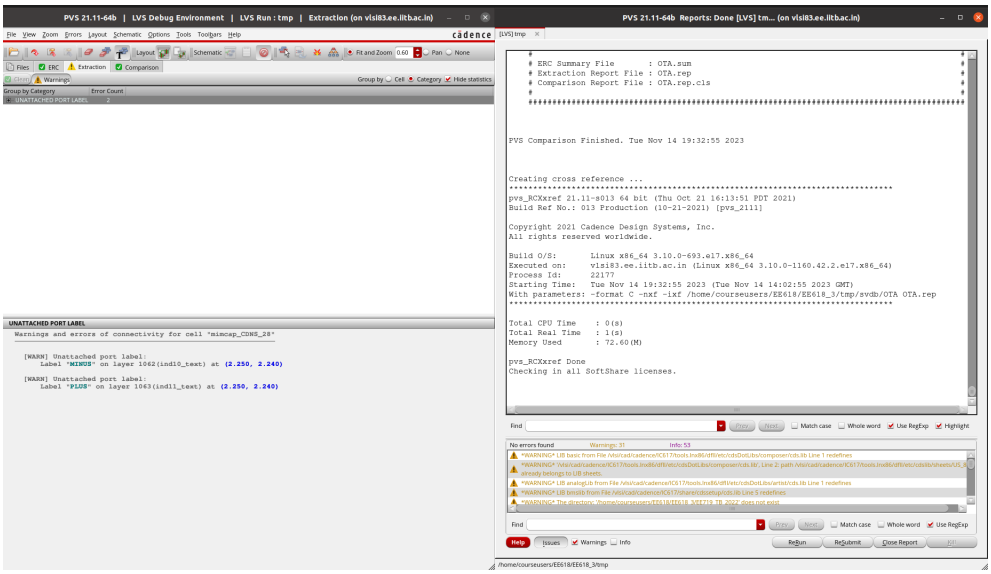

Figure 18: LVS checks for the OTA layout.

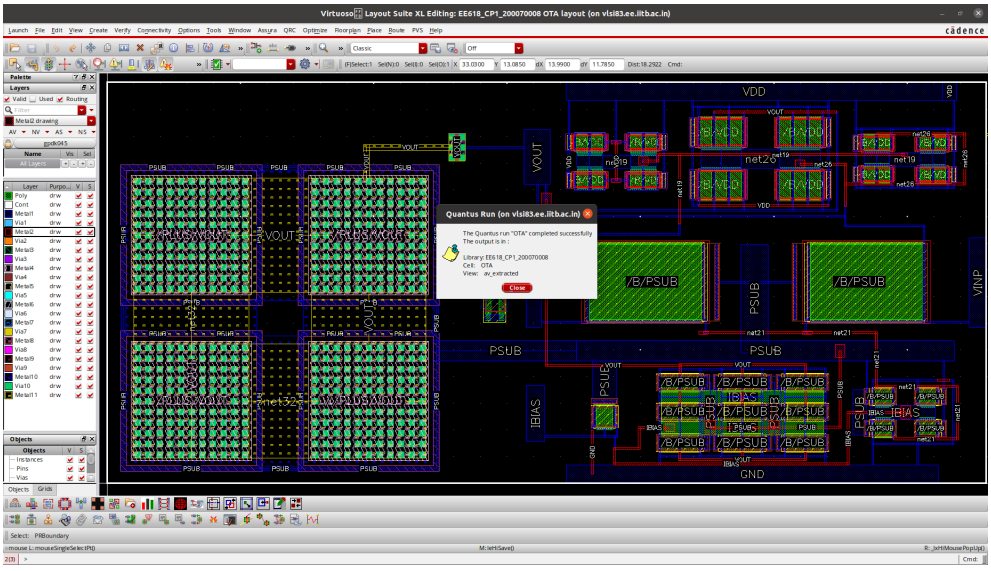

Figure 19: Quantus Run for the OTA layout.

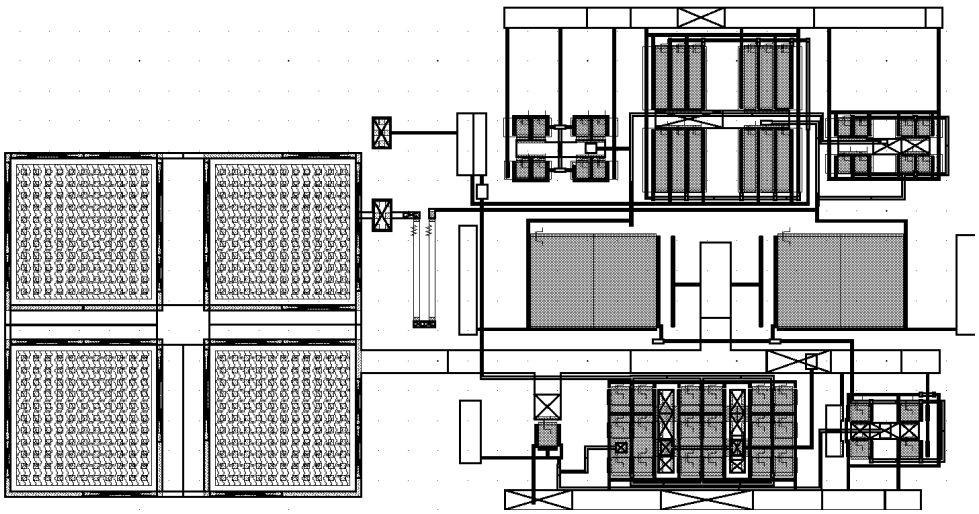

Figure 20: Layout of the OTA after parasitic extraction.

11 Layout - DC Operating point

Figure 21 shows the DC Operating point values for all the MOSFETs used after parasitic extraction. Here, we can see that all the MOSFETs are in region 2, i.e., saturation.

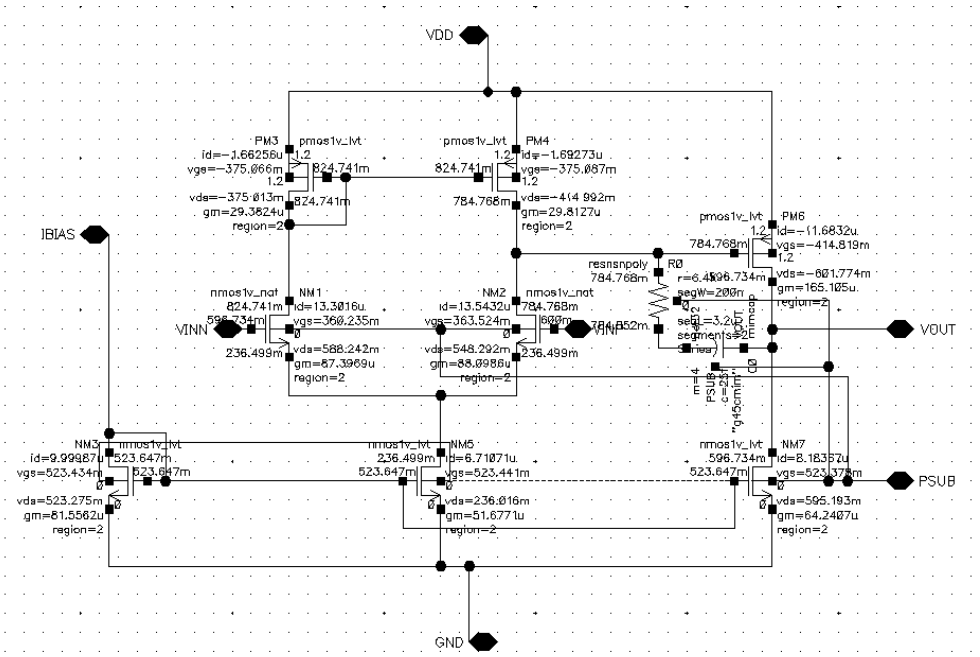

Figure 21: Schematic with DC operating point annotations after parasitic extraction.

The power consumption can be given by

$$\text{Power} = V_{DD} \times (I_{BIAS} + I_{SS} + I_{OSS}) = 1.2V \times 25\mu A = 0.03mW$$

12 Layout - Stability Analysis

Figure 22 shows the Bode plot for Gain and Phase. Here, we can observe a **DC Gain of 50.4dB**, a **3dB frequency of around 323kHz**, a **unity gain frequency of 108MHz**, and a **phase margin of around** 70.4°. Figure 23 shows the summary of the stability analysis.

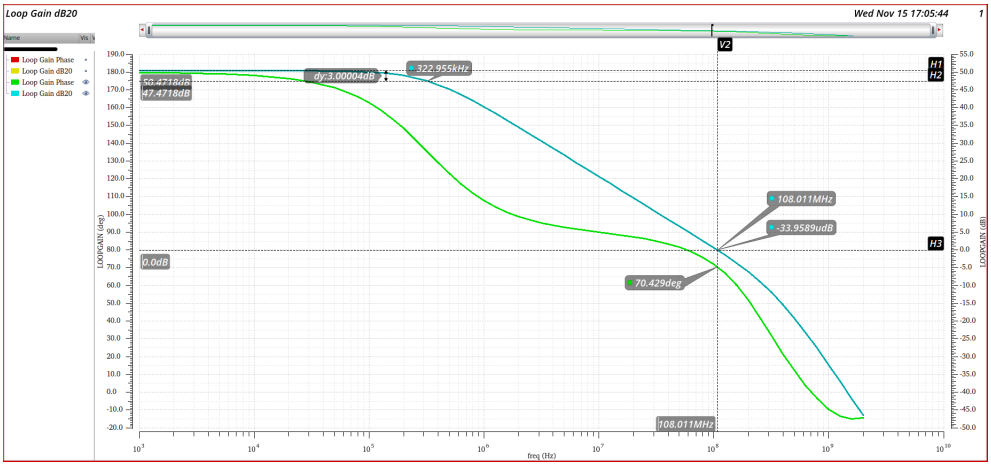

Figure 22: Bode Plots for Gain and Phase after parasitic extraction.

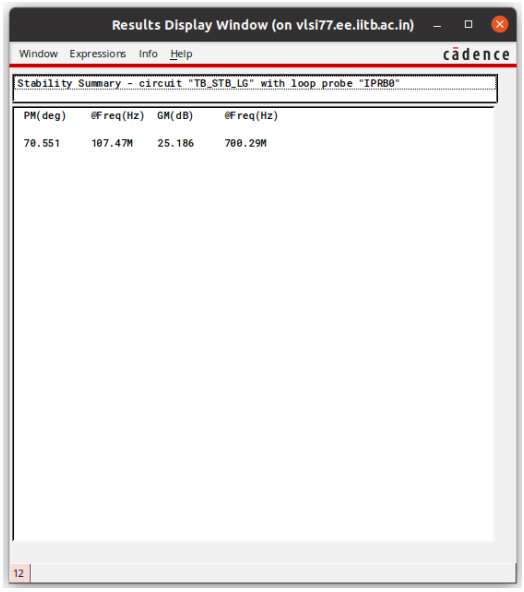

Figure 23: Stability summary after parasitic extraction.

13 Layout - AC Analysis: Differential gain

Figure 24 shows the plot for closed-loop gain and phase. We can observe the **closed-loop gain of around -7mdB** and a **3dB frequency of around 162MHz**. Figure 25 shows an **input referred systematic offset of 8.101m**. Figure 26 shows the DC Operating point values for all the MOSFETs used. Here, we can see that all the MOSFETs are still in saturation.

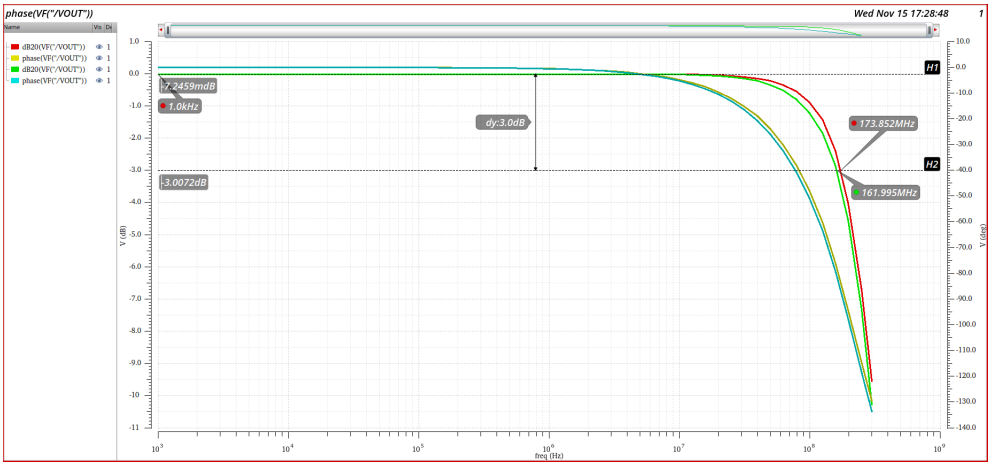

Figure 24: Bode Plots for Closed-loop Gain and Phase after parasitic extraction.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_200070008:TB_AC_DM:1	dB20(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_DM:1	phase(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_DM:1	Input reffered offset	8.101m			

Figure 25: Input referred systematic offset after parasitic extraction.

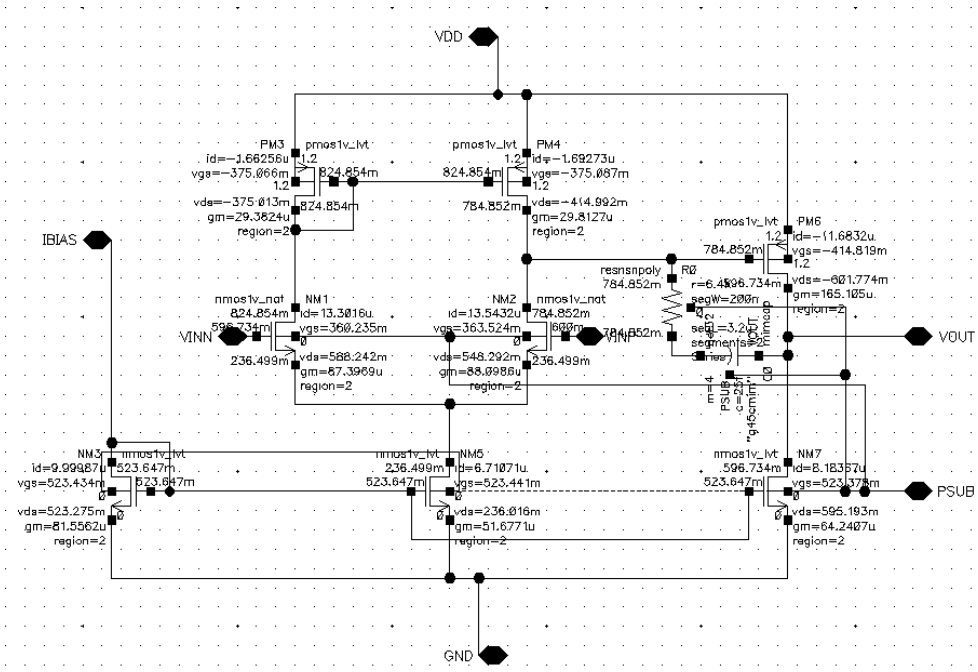

Figure 26: Schematic with DC operating point annotations after parasitic extraction.

14 Layout - DC Analysis: Common mode gain

Figure 27 shows the Bode plot for open-loop common-mode gain and phase. Figure 28 shows that the OTA has common-mode gain $A_{CM,dB} = -18.75dB$

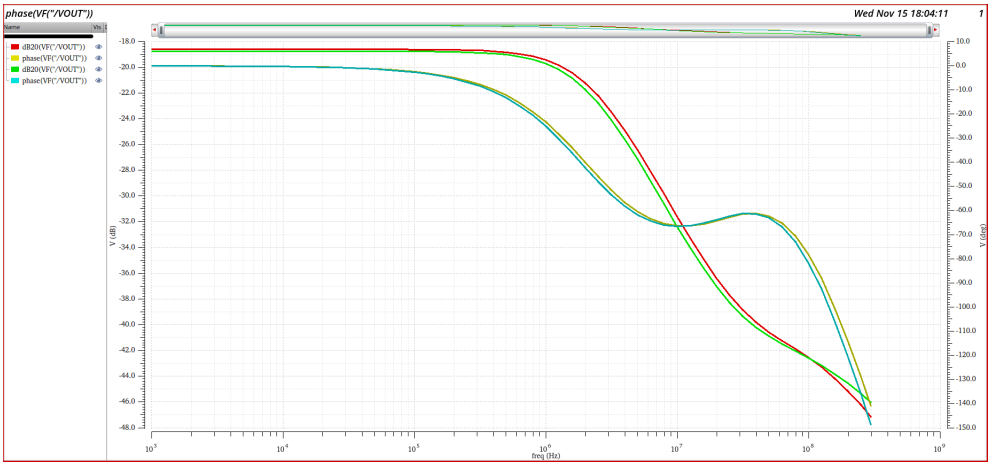

Figure 27: Bode Plots for Open-loop Common-mode Gain and Phase after parasitic extraction.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_200070008:TB_AC_CM:1	dB20(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_CM:1	phase(VF("/VOUT"))				
EE618_CP1_200070008:TB_AC_CM:1	ACM (in dB)	-18.75			

Figure 28: Common-Mode Gain after parasitic extraction.

The CMRR of the OTA is given by

$$\text{CMRR} = A_{DM,dB} - A_{CM,dB} = 50.4dB - (-18.75dB) = 69.15dB$$

15 Layout - Transient Analysis: Sinusoidal input

Figure 31 shows the plot for the input and output waveforms for the OTA after parasitic extraction. Figure 30 shows that the peak-to-peak voltage for the output waveform is around **596mV**.

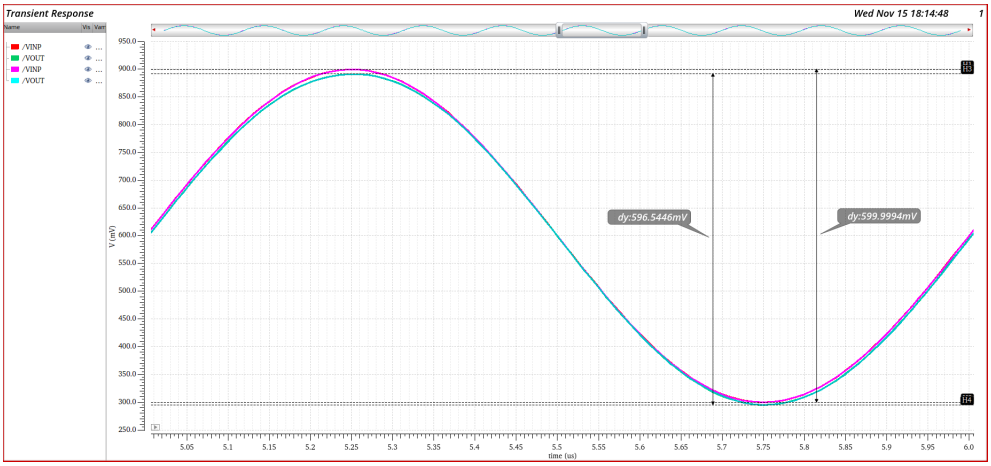

Figure 29: Plots for input and output transient waveforms after parasitic extraction.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20007 0008:TB_TRAN_SIN:1	/VOUT				
EE618_CP1_20007 0008:TB_TRAN_SIN:1	/VINP				
EE618_CP1_20007 0008:TB_TRAN_SIN:1	VOUT (peak-peak)	596m			
EE618_CP1_20007 0008:TB_TRAN_SIN:1	VIN (peak-peak)	600m			

Figure 30: Peak-to-peak voltage for input and output waveforms after parasitic extraction.

16 Layout - Transient Analysis: Step input

Figure 31 shows the plot for the input and output waveforms for the OTA to observe slewing. The slew rate is given by the following:

$$\text{Slew Rate} = \frac{\Delta V}{\Delta t} = \frac{14.15mV}{0.0867ns} = 163V/\mu s$$

The settling time can be observed to be around **6.84ns**.

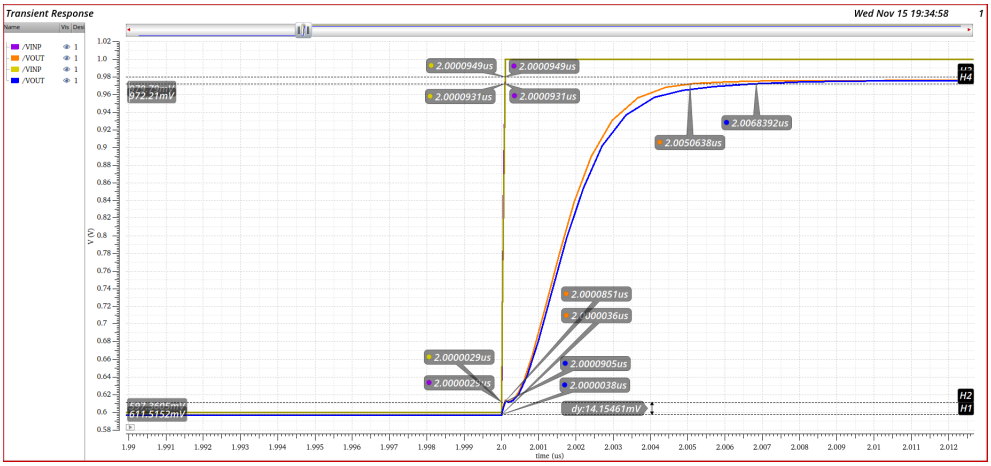

Figure 31: Plots for input and output transient waveforms to observe slewing after parasitic extraction.

17 Layout - Noise Analysis

Figure 32 shows the plot for the noise waveform. We can observe that for 1MHz, we have $\overline{V_{n,in}} = 34.5nV/\sqrt{\text{Hz}}$ and $\overline{V_{n,in}} = 30.8nV/\sqrt{\text{Hz}}$ for 10MHz frequency. Figure 33 shows the summary of the noise analysis.

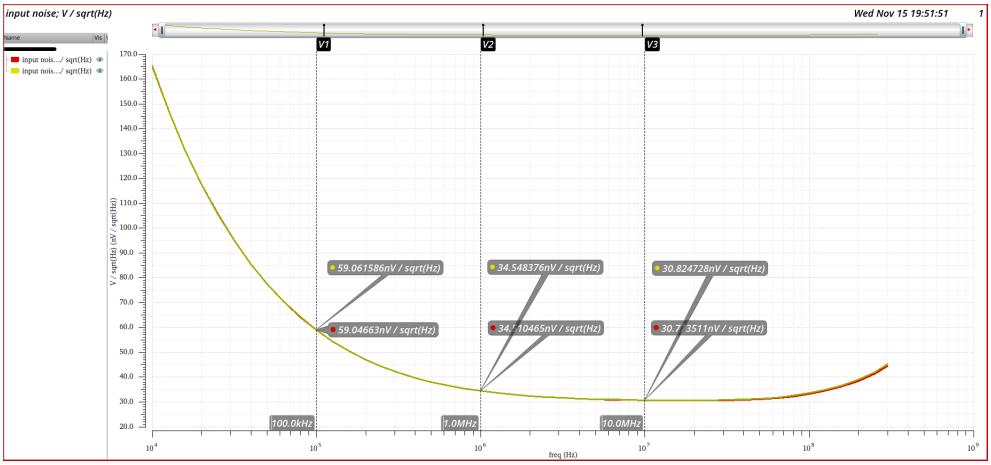

Figure 32: Plots for noise waveform after parasitic extraction.

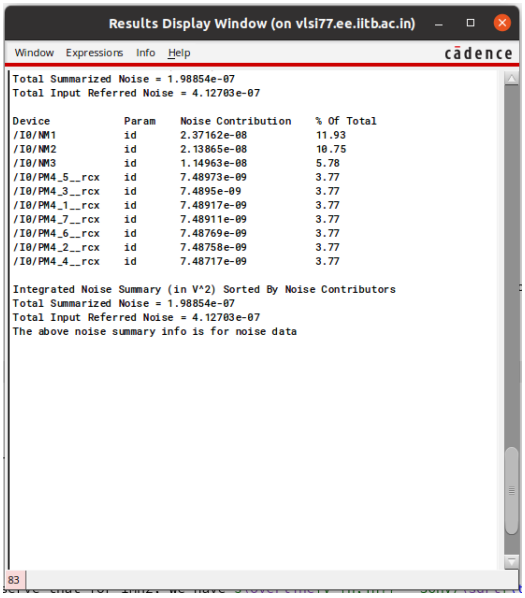

Figure 33: Noise summary after parasitic extraction.

Q. No.	Parameters	Schematic	Layout
2	Power Consumption	0.218mW	0.03mW
3	DC Gain	50.4dB	50.4dB
	f-3dB	355kHz	323kHz
	Unity gain frequency	116MHz	108MHz
	Phase Margin	68.5°	70.4°
4	Closed loop Gain	-7mdB	-7mdB
	f-3dB	174MHz	162MHz
	Input referred offset	3.208m	8.101m
5	Common mode gain	-18.6dB	-18.75dB
	CMRR	69dB	69.15dB
6	Output Swing	596mV	596mV
7	Slew rate	173V/μs	163V/μs
	Settling time	5.06ns	6.84ns
8	Input referred spot noise (at 1MHz)	34.5nV/$\sqrt{\text{Hz}}$	34.5nV/$\sqrt{\text{Hz}}$
	Input referred spot noise (at 10MHz)	30.8nV/$\sqrt{\text{Hz}}$	30.8nV/$\sqrt{\text{Hz}}$
	Total summarized noise	2.1×10^{-7}	1.99×10^{-7}
	Total input referred noise	4.02×10^{-7}	4.13×10^{-7}

Table 3: Summary of the OTA specifications.

18 Observations

Below are my observations and comments regarding the differences between the schematic and post-layout simulation results:

- Smaller bias currents (and reduced power consumption) due to the IR voltage drop.
- Slight reduction in the 3dB frequency and the unity-gain frequency due to the extra non-dominant poles introduced by the parasitic capacitance.
- Slight increase in the phase margin due to a smaller unity-gain frequency.
- Increased input-referred offset voltage due to MOSFET mismatches.
- Reduction in the slew rate due to parasitic capacitance.
- Increase in the settling time due to a larger time constant (proportional to $R \times C$).
- The noise contribution from resistive elements has increased.